REMARKS

Claims 8, 15 and 23-38 are all the claims presently pending in the application. Claims 8, 15, 23, 29 and 31-35 have been amended to more particularly define the invention. Claim 36-38 have been added. Attached hereto is a marked-up version of the changes made to the specification and claims by the current Amendment.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 8, 15 and 23-35 stand rejected under 35 U.S.C. § 112, first paragraph. Claims 8, 15, 23-27, 29-32 and 34-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zheng (US Patent No. 5,728,621) in view of Liao (US Patent No. 6,110,795) and Philipossian (US Patent No. 5,316,965). Claims 28 and 33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zheng in view of Liao and Philiposian and further in view of Brewer (US Patent No. 6,322,600).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor substrate having a trench region including at least one trench, the trench having a single layer of non-nitrided seamless filler material having an unpolished upper surface, and a non-trench region having an upper surface which is substantially co-planar with the unpolished upper surface of the single layer of non-nitrided seamless filler material.

Conventional substrates having shallow trench isolation (STI) regions require harsh reactive ion etching (RIE) or chemical mechanical polishing (CMP) to planarize the surface of the substrate and filler material formed in trenches in the substrate. However, this results in the upper surface of the filler material having scratches and chatter marks which may affect the performance of an active device formed in the substrate.

The claimed substrate, on the other hand, includes a trench region having at least one trench with a single layer of non-nitrided seamless filler material. Moreover, the claimed substrate includes a non-trench region having an upper surface which is substantially co-planar with the unpolished upper surface of the single layer of the non-nitrided seamless filler material. This structure helps to ensure that the performance of an active device formed in the substrate is not adversely affected, for example, by the surface of the trench regions.

II. THE 35 U. S. C. 112, FIRST PARAGRAPH REJECTION

The Examiner alleges that claims 8, 15 and 23-35 contain subject matter which was not adequately described in the original specification. Specifically, the Examiner alleges that the specification does not disclose a substrate having a planarized surface. Applicant submits, however, that these claims are adequately supported by the specification.

Specifically, Applicant notes that the Application provides that the invention is related to "planarized shallow trench isolation structures" (page 1, lines 5-6). It is explained that it has become common "to form trench isolation regions nominally co-planar with adjoining active semiconductor regions of semiconductor substrates (page 1, lines 15-20), and that trench regions "nominally co-planar with active semiconductor regions within semiconductor substrates are desirable" (page 2, lines 3-5). In addition, Figure 6 of the Application is said to illustrate a "planarized STI structure" and that further processing "results in the fully planarized structure depicted in Figure 7" (page 12, lines 9-12).

Applicant also notes that the fact that the upper surface in the non-trench region and the upper surface of the filler material in the trench may be planarized is clear from the description of the process which may be used to form the substrate which is described in the Application. Specifically, referring to Figure 1, it is explained that the oxide material 50b in the trench should be "slightly thicker than the depth of the trench region 20" (page 6, lines 7-8). It is later explained that a small portion of this oxide material 50b may be removed by an etch process (page 8, lines 4-5). Thus, Applicant submits that if the material 50b in the trench is only "slightly thicker" than the depth of the trench, and a small portion of the material 50b is removed by a etching process, it is clearly that the upper surface of the filler material is

substantially co-planar with the upper surface of the substrate in the non-trench region.

Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. THE PRIOR ART REFERENCES

A. The Zheng, Liao and Philiposian References

The Examiner alleges that Zheng would have been combined with Liao and Philiposian to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Zheng discloses a method for forming planarized oxide shallow trench isolation. In the Zheng method, a high density plasma (HDP) oxide layer is deposited in the isolation trenches. A layer of spin-on-glass is coated over the HDP oxide layer. The spin-on-glass layer and portions of the HDP oxide layer remaining are polished away so that the substrate is planarized (Zheng at Abstract).

Liao discloses an method of fabricating a shallow trench isolation. In the Liao method, a trench is formed an an isolation layer is formed to fill the trench. The isolation layer is planarized by chemical mechanical polishing with the hard mask layer as an stop layer, so that a micro-scratch is formed on a surface of the isolation within the trench. A sacrificial layer is formed on the isolation layer and the hard mask layer. The micro-scratch is thus filled with the sacrificial layer. Using the hard mask as an etch stop, the sacrificial layer is etched back. Since the etching rate of the sacrificial layer is the same as or lower than the isolation layer within the trench, the formation of the micro-scratch is suppressed during the etching back process (Liao at Abstract).

Philiposian discloses a process for planarizing an isolation barrier. The process involves reducing the etch rate of the field oxide by nitriding the field oxide independently of the sacrificial oxide layer (Philiposian at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters. Specifically, Zheng planarizes a substrate surface by chemical mechanical polishing (CMP),

and Laio teaches that CMP damages a substrate surface and planarizing the substrate surface by filling the damaged areas (e.g., microscratches) (Laio at col. 1, lines 13-17), whereas Philiposian allegedly planarizes a substrate surface by nitriding the field oxide layer independent of the sacrificial oxide layer. Clearly, these references teach away from each other so that no person of ordinary skill in the art would have considered combining the references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that "[o]ne skilled in the requisite art ... would choose the removal method taught by Zheng that will result in a substantially scratch free surface as taught by Laio and to a co-planar surface with the substrate as taught by Philipossian" which is insufficient to support the combination.

Moreover, contrary to the Examiner's allegations, none of these references teach or suggest "a trench region comprising at least one trench, said trench comprising a single layer of non-nitrided seamless filler material having an unpolished upper surface" and "a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said non-nitrided seamless filler material" as recited in claim 8 and similarly recited in claims 15 and 23.

As noted above, conventional substrates having shallow trench isolation (STI) regions require harsh reactive ion etching (RIE) or chemical mechanical polishing (CMP) to planarize the surface of the substrate and filler material formed in trenches in the substrate (Application at page 2, lines 9-18). However, this results in the upper surface of the filler material having scratches and chatter marks which may affect the performance of an active device formed in the substrate.

The claimed substrate, on the other hand, includes a trench region having at least one trench with a single layer of non-nitrided seamless filler material (Application at page 6, lines7-15; Figure 7). Further, the claimed substrate includes a non-trench region having an upper surface which is substantially co-planar with the unpolished upper surface of the single layer of the non-nitrided seamless filler material (Application at page 12, lines 9-12; page 13,

lines 1-3). This structure helps to ensure that the performance of an active device formed in the substrate is not adversely affected, for example, by the surface of the trench regions.

More specifically, the claimed substrate may be formed using a novel method which eliminates the need for RIE and CMP in order to planarize the substrate and trench regions. As explained in the Application, the novel method may include forming a trench in a substrate, and forming a pad nitride on an upper surface of the substrate (Application at Figure 1). A non-conformal filler material (e.g., high density plasma oxide) may be used to fill a trench (Application at page 5, line 19-page 7, line 19).

Importantly, the filler material may be etched slightly to expose a portion of the pad nitride near the trench (Application at Figure 2; page 7, line 20-page 8, line 9), and a photoresist formed over the trench region to protect the filler material in the trench (Application at Figure 3; page 8, line 10-page 9, line 10). The filler material remaining on the pad nitride may then be etched away, while the filler material in the trench is not etched (Application at Figure 4). The photoresist and pad nitride may then be removed resulting in the planarized structure shown in Figure 7 (Application at page 9, line 9-page 10, line 10).

Applicant respectfully submits that this novel method of forming the claimed substrate results in the novel features of the claimed invention, including a single layer of non-nitrided seamless filler material with an upper surface which is unpolished and substantially coplanar with a substrate surface. Further, Applicant respectfully submits that without using the novel method described in the Application it would be likely be impossible to form a substrate having these novel features.

Clearly, the references do not teach or suggest these novel features. First, Zheng does not use this novel method of forming the claimed substrate, and therefore, it is unlikely that Zheng can form this novel structure. For instance, Zheng teaches going immediately from the structure of Figure 5 to the structure of Figure 6 by chemical mechanical polishing. In other words, Zheng does not include the steps of etching the filler material slightly to expose a portion of the pad nitride near the trench, then protecting the filler material in the trenches and etching away the filler material on the nitride pad. Therefore, Applicant submits that it is unlikely that Zheng can form the claimed substrate.

More particularly, Zheng specifically teaches chemical mechanical polishing in order to planarize the STI region (Zheng at col. 3, lines 22-26). The Examiner alleges that Zheng teaches that the etching may be optionally used to planarize the surface. However, Applicant respectfully submits that the Examiner is misreading Zheng.

Specifically, it may be "optional" to form the CMP step described at col. 3, lines 21-26 in Zheng. However, if CMP is not performed the resulting structure will appear as the structure depicted in Figure 5. In other words, Zheng teaches only one method for achieving the planarized structure shown in Figure 6, and that is by using CMP (Zheng at col. 3, lines 21-25 and lines 64-66).

Indeed, specifically states that a CMP step is need to achieve a planarized structure. For example, it is stated that "[t]he spin-on-glass layer and HDP oxide layer remaining are polished away wherein the substrate is planarized" (Zheng at Abstract). Further, Zheng states that after the etch-back step about 2000 to 3000 Angstroms of HDP oxide remains on the nitride pad and that "Figure 5 illustrates the wafer after etchback" (Zheng at col. 3, lines 19-20). Therefore, Zheng clearly teaches a filler material having a polished surface which is contrary to the claimed invention.

Likewise, Laio does not teach or suggest the novel features of the claimed invention. Indeed, Laio teaches merely forming an oxide layer in a trench and on a mask layer 24 to form an isolation layer 30. Then Laio uses CMP to planarize the isolation layer, forms a sacrificial layer to fill in the microscratches formed by the CMP, then planarizes the surface by etching (Laio at col. 2, lines 53-60; Figure 2E). In other words, Laio requires multiple layers of filler material to planarize the substrate surface.

However, this is completely different from the claimed invention which may use a single layer of seamless filler material to provide a surface which is substantially co-planar with the substrate surface in a non-trench region. In other words, Laio may disclose a filler material having a planarized upper surface, however, it is not the upper surface of a "single layer" in the trench. Therefore, Laio does not make up for the deficiencies of Zheng.

Similarly, Philipossian does not make up for the deficiencies of Zheng and Laio. As noted above, Philiposian allegedly planarizes a substrate surface by nitriding the field oxide

layer independent of the sacrificial oxide layer. However, the claimed invention includes a filler material which is non-nitrided (Application at page 5, line 19-page 6, line 2).

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Brewer Reference

The Examiner alleges that Brewer would have been combined with Zheng, Laio and Philipossian to form the claimed invention. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Brewer discloses a planarization composition for chemical mechanical planarization of dielectric layers for semiconductor manufacture, and methods for using the planarization composition in the manufacture of semiconductor devices (Brewer at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters. Specifically, Zheng planarizes a substrate surface by chemical mechanical polishing (CMP), Laio teaches that CMP damages a substrate surface and planarizing the substrate surface by filling the damaged areas (e.g., microscratches) (Laio at col. 1, lines 13-17), and Philiposian allegedly planarizes a substrate surface by nitriding the field oxide layer independent of the sacrificial oxide layer, whereas Brewer is merely directed to a planarization composition for CMP (Laio at col. 1, lines 13-17). Therefore, no person of ordinary skill in the art would have considered combining these references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that "[o]ne skilled in the requisite art ... would modify Zhang by adding dopant to the oxide trench fill as suggested by Brewer with reasonable expectation of producing a trench fill of a desired dielectric constant" which is

insufficient to support the combination.

Further, Applicant notes that it is not Zheng that the Examiner must show would have been modified by Brewer's teachings. Instead, the Examiner must show that the combination of Zheng, Laio and Philipossian would have been modified by Brewer. This the Examiner has failed to do.

Moreover, like the other references, Brewer does not teach or suggest "a trench region comprising at least one trench, said trench comprising a single layer of non-nitrided seamless filler material having an unpolished upper surface" and "a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said non-nitrided seamless filler material" as recited in claim 8 and similarly recited in claims 15 and 23.

As noted above, unlike conventional substrates with planarized STI regions, the claimed substrate includes a trench region having at least one trench with a single layer of non-nitrided seamless filler material (Application at page 6, lines7-15; Figure 7). Further, the claimed substrate includes a non-trench region having an upper surface which is substantially co-planar with the unpolished upper surface of the single layer of the non-nitrided seamless filler material (Application at page 12, lines 9-12; page 13, lines 1-3). This structure helps to ensure that the performance of an active device formed in the substrate is not adversely affected, for example, by the surface of the trench regions.

More specifically, the claimed substrate may be formed using a novel method which eliminates the need for RIE and CMP in order to planarize the substrate and trench regions.

Clearly, Brewer does not teach or suggest these novel features. Indeed, Brewer is merely directed to a composition for chemical mechanical polishing and is unrelated to the claimed substrate.

Specifically, Brewer may disclose a trench region in a substrate (Brewer at Figure 7b). However, the whole point of Brewer is to improve a CMP process for forming a trench region (Brewer at col. 11, line 40- col. 12, line 22). Applicant notes that it is very unlikely that any person of ordinary skill in the art would rely upon Brewer whose primary objective is to improve a CMP process, to form the claimed invention which may be formed without CMP.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 8, 15 and 23-38, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: 11/20/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims to read as follows:

8. (Thrice Amended) A semiconductor substrate comprising:

a trench region comprising at least one trench, said trench comprising a single layer of non-nitrided seamless filler material having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially [unpolished and] co-planar with said unpolished [a] upper surface of said single layer of said non-nitrided seamless filler material [substrate].

15. (Thrice Amended) A semiconductor substrate [having a planarized trench region formed according to a method] comprising:

a trench region comprising at least one trench, said trench comprising a single layer of non-nitrided seamless high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said non-nitrided seamless HDP oxide

[forming a pad on a surface of said substrate;

forming at least one trench in said substrate;

applying a seamless filler material by high density plasma method in said at least one trench and on said pad;

selectively removing said filler material on said pad so as to separate said filler material in said at least on trench and said filler material on said surface by an exposed area of said pad,

removing said filler material on said pad,

wherein said filler material has an upper surface which is unpolished and co-planar with a upper surface of said substrate].

23. (Four Times Amended) A semiconductor substrate [having a planarized structure formed according to a method] comprising:

a trench region comprising a plurality of trenches, each of said trenches comprising a single layer of non-nitrided seamless high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said non-nitrided seamless HDP oxide,

wherein said upper surface of said non-trench region comprises implanted dopants

[forming a pad on a surface of said substrate;

forming at least one trench in said substrate;

applying a seamless filler material by high density plasma method in said at least one trench and on said pad, said filler material filling at least a portion of said at least one trench;

selectively removing said filler material on said pad so as to separate said filler material in said at least on trench and said filler material on said surface by an exposed area of said pad, and

removing said filler material on said pad while allowing said filler material in said at least a portion of said at least one trench to remain,

wherein said filler material has an upper surface which is unpolished and co-planar with a upper surface of said substrate].

29. (Twice Amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of non-nitrided seamless filler material and said upper surface of said non-trench region [substrate] are planarized without reactive ion etching.

31. (Amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of non-nitrided seamless filler material and said upper surface of said non-trench region [substrate] are planarized without chemical mechanical polishing.

32. (Amended) The semiconductor substrate according to claim 8, wherein said upper

surface of said single layer of non-nitrided seamless filler material is substantially scratch-free.

33. (Amended) The semiconductor substrate according to claim 8, wherein said upper surface of said non-trench region [substrate] comprises implanted dopants.

34. (Amended) The semiconductor substrate according to claim 8, further comprising:
a thin oxide layer grown on said upper surface of said non-trench region [substrate].

35. (Amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of seamless filler material is free of chatter marks.